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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/062,044
	Filing Date	1/31/02
	First Named Inventor	Steven Teig, et al.
	Group Art Unit	2825
	Examiner Name	N. Levin
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0093

Enclosures (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm Or Individual name	Gregory Suh, Reg. No. 48,187 of Stattler Johansen & Adeli LLP
Signature	
Date	March 23, 2004

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PATENT
Docket No. SPLX.P0093

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Gregory Suh

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/062,044

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PRODUCING A CIRCUIT
DESCRIPTION OF A DESIGN

**INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97**

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Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

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Dated: March 23, 2004

Respectfully submitted,

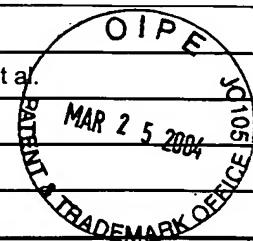
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/062,044
				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	N. Levin
Sheet	1	of	3	Attorney Docket Number	SPLX.P0093



U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document		Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	1.	2002/0157063	A1	10-24-2002	Besson	
	2.	2002/0178432	A1	11-28-2002	Kim et al.	
	3.	2003/0145288	A1	07-31-2003	Wang et al.	
	4.	4,703,435		10-27-1987	Darringer et al.	
	5.	5,003,487		03-26-1991	Drumm et al.	
	6.	5,521,835		05-28-1996	Trimberger	
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	9.	5,892,678		04-06-1999	Tokunoh et al.	
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	12.	6,035,107		03-07-2000	Kuehlman et al.	
	13.	6,080,204		06-27-2000	Mendel	
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	16.	6,334,205		12-25-2001	Iyer et al.	
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	21.	6,453,447	B1	09-17-2002	Gardner et al.	

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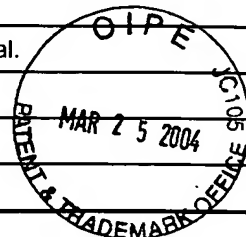
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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	N. Levin
Sheet	2	of	3	Attorney Docket Number	SPLX.P0093



U.S. PATENT DOCUMENTS						
	22.	6,470,478	B1	10-22-2002	Bargh et al.	
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	24.	6,496,972	B1	12-17-2002	Segal	
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	31.	6,574,779	B2	06-03-2003	Allen et al.	
	32.	6,618,835	B1	09-09-2003	Garlapati et al.	

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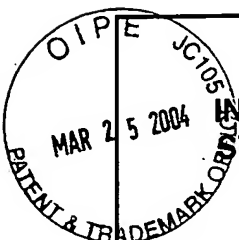
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				Filing Date 1/31/02
				First Named Inventor Steven Teig, et al.
				Group Art Unit 2825
				Examiner Name N. Levin
Sheet	3	of	3	Attorney Docket Number SPLX.P0093

NON PATENT LITERATURE DOCUMENTS				
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ⁶
	33.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).		
	34.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vo.. 37, No. 11, pp. 291-292 (4 pages).		
	35.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargeting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics", Vol. 2, 14 May 2000, pp. 703-706.		
	36.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.		
	37.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.		
	38.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol.2, August 1997.		

Examiner Signature	Date Considered
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